

In-system programming

PXI Express: Overkill for JTAG/Boundary Scan Equipment?

By Heiko Ehrenberg

Well established as a valuable test and debug access methodology, JTAG/Boundary Scan as defined in IEEE 1149.1 can be implemented in test systems based on various hardware platforms. Heiko explores whether a high speed tester platform such as PXI Express provides benefits for structural test and in-system programming applications based on JTAG / Boundary Scan access.

Just as PXI was developed as an extension of PCI to satisfy special requirements in the test and measurement industry, PXI Express [1] is based on PCI Express [2] and provides respective extensions to that standard. Because of that tight relationship, future improvements in PCI Express will be available in PXI Express, too. The PXI Express specification, approved in August 2005, is maintained by the PXI System Alliance.

PXI Express has been developed in order to allow the creation of state-of-the-art test systems with the highest system throughput, in application areas such as real-time RF or video processing. However, other test and measurement applications can benefit from this gain in system throughput as well. Applications that have been available only in PCI Express realm can now be realized in the PXI form factor by means of PXI Express systems.

Why Boundary Scan based on PXI Express?

Some JTAG/Boundary Scan [3] applications, such as in-system programming of FLASH devices, memory cluster testing of complex memory devices, and functional test applications utilizing Boundary Scan cells, for example to capture logic values on specific pins or to stimulate nets or device internal resources, can require enormous throughput. To satisfy this throughput, the tester hardware platform needs to provide the appropriate bandwidth, something especially serial bus systems such as USB (maximum throughput 480 MBps), but also parallel platforms such as PCI (127 MBps¹) may have problems with.

PXI Express combines the benefits of a modular platform featuring test specific capabilities not available in a PC based environment with the high-performance bandwidth of the PCI Express bus. This enables the creation of powerful but compact, flexible automated test systems that combine the versatility of functional test equipment with the embedded test access and diagnostic capabilities of Boundary Scan. Integrating functional test and

Boundary Scan access in a PXI Express environment enables new test, debug, and emulation applications.

JTAG/Boundary Scan has been implemented in PXI based test equipment for many years. See Figure 1 (next page) for Goepel's Boundary Scan controller. The actual speed improvement for Boundary Scan applications gained from the additional bandwidth provided by PXI Express depends on the Boundary Scan controller performance, the type of Boundary Scan application, and the Boundary Scan resources on the Unit Under Test (UUT). PXI Express provides up to 2 GBps dedicated bandwidth per slot, which a PXI Express based Boundary Scan controller could take advantage of. Due to the software compatibility between PXI and PXI Express, upgrading a PXI system to a PXI Express based test system should be effortless.

An application example

Let us look at an example UUT: a board design contains six Boundary Scan devices (Table 1), two SDRAM devices, four DDR2 SDRAM devices, two FLASH EEPROM devices (16 x 2 Mb), several buffers and simple logic gates, and a variety of passive components. For this analysis we will look at in-system programming of FLASH devices particularly.

Device type	Package	BSR ² length	TCK _{max} [MHz]
CPU	CBGA552	769	20
DSP	BGA240	302	25
PLD	BGA256	624	10
PLD	FBGA256	480	10
FPGA	BGA600	1308	10
FPGA	FBGA484	1446	10

Table 1

¹ 32 bit / 8 bit * 33.3 MHz * 1,000,000 / 1,048,576 = 127 MBps

² BSR = Boundary Scan Register

“ Even though the numbers given are only representative for specific types of applications, it becomes obvious that PXI Express can provide a dramatic improvement in throughput for data intensive Boundary Scan applications. ”

If all Boundary Scan compliant devices are connected in one scan chain, the total number of Boundary Scan cells in the scan chain is 4,929 cells. The maximum TCK frequency is 10 MHz (the slowest device in the chain determines the maximum TCK frequency; in reality the maximum TCK may be even less if the scan chain is not designed well). Based on these numbers, it takes about 493 microseconds to shift through the Boundary Scan chain, ignoring any software or hardware overhead. With this long shift time, the maximum sample or update rate on a Boundary Scan I/O pin would be about 2 kHz. The only way to improve that throughput on the I/O pins would be to shorten the Boundary Scan chain by putting some devices in BYPASS mode.

The FLASH devices on this UUT require six shift cycles on the Boundary Scan chain to program one word. For details regarding FLASH programming through Boundary Scan please refer to [4] and [5]. The 32 Mb FLASH memory devices on the UUT are programmed in 16-bit words, requiring 2,048,000 programming cycles. Assuming that only the DSP and the CPU need to be in test mode (their Boundary Scan registers are used) and the other four devices are in BYPASS mode and in a separate scan chain, the number of bits to transmit per shift cycle is 1,072 bits (302 + 769) and the maximum TCK frequency is 20 MHz. The shift time for each vector would be 53.6 microseconds. Total shift time t_{shiftT} would be 658.64 seconds:

$$t_{\text{shiftT}} = 53.6 \mu\text{s} * 6 * 2,048,000 = 658.64 \text{ s}$$

The total amount of data to be transmitted $\text{DATA}_{\text{transmit}}$ would be 13 Gb:

$$\text{DATA}_{\text{transmit}} = 1,072 \text{ bit} * 6 * 2,048,000 = 13,172,736,000 \text{ bit}$$

Dealing with the overhead

This amount of data will impose a noticeable overhead on the execution time of the FLASH programming application.

PCI (and PXI) has a bandwidth of 127 MBps, or approximately 1 Gbps. In practice, it takes sometimes more than one PCI cycle to transmit 32 bits, so the effective throughput would be less than 1 Gbps. Even so, the overhead for data transmission $\text{overhead}_{\text{PCI}}$ would be only about 2% of the shift time needed under the conditions mentioned above:

$$t_{\text{PCItransmit}} = 13 \text{ Gb} / 1 \text{ Gbps} = 13 \text{ seconds}$$

$$\text{overhead}_{\text{PCI}} = 13 \text{ s} * 100\% / 658.64 \text{ s} = 2\%$$

PCI Express (and PXI Express) has a bandwidth of 2.5 Gbps in a x1 link. Assuming that in practice the effective bandwidth for the transmission of the Boundary Scan vectors would be more like 2 Gbps, this would still mean an improvement of 100% compared to PCI/PXI, resulting in an overhead of only about 1% of the shift time in this application example.

This overhead becomes more noticeable, the faster the TCK gets. For example, for a TCK of 100 MHz, the transmission of data over the host bus would be 10% and 5% for PCI/PXI and PCI Express/PXI Express, respectively.

In practice, one byte often times transmits only one TCK cycle on the host bus (the actual amount of data required to transmit one TCK cycle from the tester software to the UUT depends on the Boundary Scan controller implementation). This would mean that a 32 bit PCI cycle does not transmit 32 TCK clocks, but only 4, effectively reducing the throughput to 130 Mbps – referred to as *Effect A* below. This would result in a data transmission overhead of about 16% for PCI with a TCK on the UUT of 20 MHz. For a x1 PXI Express link the overhead can be scaled in a similar way to approximately 8%.

On the other hand, considering that PCI typically requires two clocks to transmit one write cycle, and even more – up to 10 clocks – for one read cycle (referred to as *Effect B* below), the data transmission overhead on a PCI based test system would increase in the neighborhood of 4% to 20% of the shift time on the UUT. This effect is only true for PCI signaling, not for PCI Express.

When combining the impact of Effect A and Effect B, the actual overhead for data transmission on PCI compared to shift time on the UUT lies somewhere between 64% and 320%, compared to about 8% for a PCI Express (or PXI Express) x1 link for this application example. So, in real world implementations, the host bus bandwidth can have a big impact on the run time of data intensive Boundary Scan applications such as in-system programming of FLASH devices. Table 2 compares the data transmission times for PXI and PXI Express platforms.

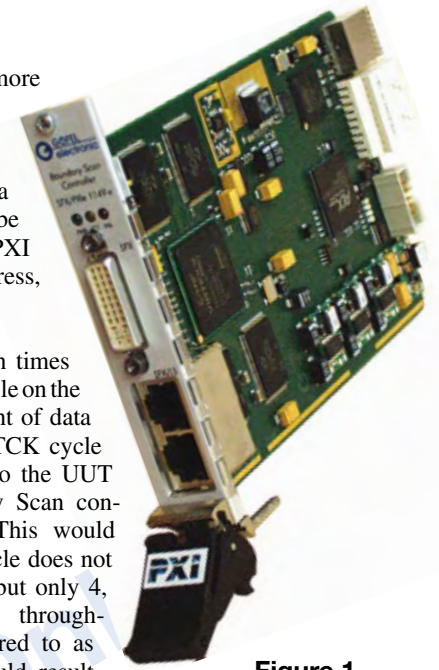


Figure 1

Host bus, effective bandwidth	Data packet size [byte]	Frame size [byte]	Data to be transmitted [GB]	Minimum transmission time [sec]
PXI 500 Mbps	1	4	1,6	105
PXI Express x1 2 Gbps	4096	4124	1,6	7

Table 2

Even though the numbers given are only representative for specific types of applications, it becomes obvious that PXI Express can provide a dramatic improvement in throughput for data intensive Boundary Scan applications.

Faster for data intensive applications

For many Boundary Scan applications, the performance of PCI/PXI is sufficient. However, data intensive application such

as in-system programming of FLASH devices can benefit from the higher bandwidth provided by PXI Express. We can expect Boundary Scan compliant devices to become faster and to offer more advanced test features in the future. This development and the migration of functional test applications into the Boundary Scan domain will generate demand for automated test equipment featuring the modularity, versatility, and bandwidth of PXI Express. **PXI**

References:

- [1] PXI Express Specifications, PXI-5 – PXI Express Hardware Specification, PXI-6 – PXI Express Software Specification, 2005, PXI System Alliance, <http://pxisa.org/specs.htm>
- [2] PCI Express Specification, PCI-SIG, <http://www.pcisig.com/specifications/pciexpress/>
- [3] IEEE Computer Society, IEEE Standard Test Access Port and Boundary Scan Architecture - IEEE Std. 1149.1 2001, Annex B, IEEE, New York, NY, 2001
- [4] Heiko Ehrenberg, White Paper: Boundary Scan Tutorial, GOEPEL Electronics, 2003
- [5] Heiko Ehrenberg, White Paper: Design-For-Testability Guidelines for Boundary Scan Test, GOEPEL Electronics, 2004

Heiko Ehrenberg received his BSEE from the University of Applied Science at Mittweida, Germany, in 1996. The same year he started with GOEPEL electronic GmbH in Germany as an applications engineer for JTAG/boundary scan. In 1998, Heiko was transferred to GOEPEL's US subsidiary. In 1999 he was promoted to managing director of operations at GOEPEL Electronics LLC in Austin, TX, which is responsible for the company's operations in the USA, Canada, and Mexico.

**GOEPEL electronics LLC****9600 Great Hills Trail, Suite 150 W****Austin, TX 78759****Tel: 512-502-3010****Fax: 512-502-3076****Email: h.ehrenberg@goepel.com****Website: www.goepel.com**